changing a process of the CPU executing the first program to a process for executing a second program stored in a mask ROM, which is formed in the semiconductor substrate, when a jump instruction in the first program is executed by the central processing unit;

executing the second program by the central processing unit to perform writing to the electrically programmable ROM by the central processing unit executing the second program; and

changing the process of the central processing unit executing the second program to the process for executing the first program when a return instruction in the second program is executed by the central processing unit,

wherein the mask ROM and the electrically programmable ROM are disposed in mutually different addresses in one address space of the central processing unit.

REMARKS

Claims 21-30 are pending and claims 21, 23, 24, 28, 29 and 30 have been amended.

Claims 21, 22, 24, 25 and 27-30 stand rejected under 35 U.S.C. §102 as being anticipated by Ugon. Claims 23 and 26 stand rejected under 35 U.S.C. §103 as being unpatentable over Ugon. Reconsideration of these rejections is requested in view of the foregoing amendments. Entry of the foregoing amendments is requested in view of the CPA that is filed

herewith. The CPA is filed to continue prosecution since the foregoing amendments to the claims would have raised a new issue and/or required further search or examination and therefore would not have been entered after the final rejection. Applicants respectfully assert that the claims as amended herein are patentable in view of the previously filed arguments against the outstanding rejections.

Applicants also submit herewith a fresh PTO-1449 form listing documents AV, AX, AY and BK that was originally filed January 29, 1999. Reconsideration of these documents is requested for the following reasons.

(1) AV: EPO 081 873 corresponds to U.S. Patent No. 4,665,480 and therefore the corresponding U.S. Patent, which is not in a foreign language can be considered. Applicants believe that a copy of the patent in electronic form is readily available to the Examiner, however, a copy will be provided if requested.

(2) AX: FR 2 430 065 corresponds to U.S. Patent No. 4,279,024, a copy of which was filed with the IDS of January 29, 1999, and which has been considered by the Examiner.

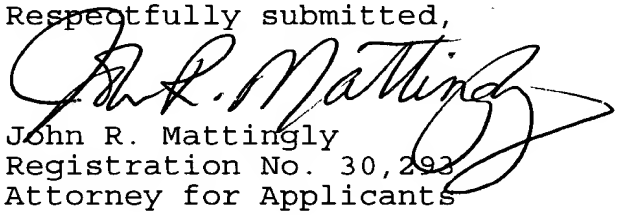
(3) AY: "Hitachi Microprocessor Data Book, 8 bit Single-Chip," pages 825 and 838-842. A copy of this document with pertinent portions of the figures thereof translated is enclosed and the following statement of relevance is provided. As disclosed in the document, the Hitachi Microprocessor HD63701X0 includes an EPROM that is shown in block diagram

form on page 825. The EPROM is capable of being programmed by an external writer when the operation mode of the Microprocessor HD63701X0 is set to an EPROM mode by applying predetermined voltages to the respective terminals MP0, MP1, /STBY, Vpp and Vss, as shown on Table 3 on page 838 and Fig. 20 on page 840. Fig. 20 on page 840 shows the memory map of the EPROM mode (in the EPROM mode, the addresses of the EPROM can only be recognized). Page 841-842 describes the programming/verifying/erasing of the EPROM in the EPROM mode.

(4) With regard to the French search report, the relevance is as set forth by the identified categories X, Y etc. of the cited references.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



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MARKED UP VERSION OF REWRITTEN CLAIMS

21. (Amended) A microcomputer comprising:

an electrically programmable ROM [which has] having:

a first [region] area to store a [user] program therein and

a second [region] area to store data therein;

a memory [which stores] storing a write control program for a writing to the electrically programmable ROM; [and]

a CPU [which executes] executing the [user] program and the write control program,

a data bus to which the CPU, the electrically programmable ROM and the memory are coupled; and

an address bus to which the CPU, the electrically programmable ROM and the memory are coupled,

wherein the electrically programmable ROM and the memory are [disposed] allocated at mutually different address [positions] space of the CPU,

wherein the [user] program includes [a first] an instruction [which changes] changing a process of the CPU [executing the user program] to a process [that controls] for controlling a [writing] programming of the electrically programmable ROM based on the write control program stored in the memory, and

[a data bus coupled to the CPU, to the electrically programmable ROM and to the memory; and

an address bus coupled to the CPU, to the electrically programmable ROM and to the memory, and]

wherein the write control program [includes] has [a second] an instruction which returns the process of the CPU to [the] a process based on the [executing of the user] program stored in the electrically programmable ROM after completion of the process that controls the writing of the electrically programmable ROM.

23. (Amended) A microcomputer according to claim 21, wherein the memory which stores a write control program is a RAM that receives the write control program from the [electrically programmable] ROM.

24. (Amended) A microcomputer comprising:

an electrically programmable read only memory (ROM) [which has] including:

a first area to store a first program therein and

a second area to store data therein;

a memory [which stores] storing a second program for controlling a writing to the electrically programmable ROM;

a central processing unit [which executes] executing the first program and the second program,

a data bus [coupled] to which the central processing unit, [to] the electrically programmable ROM and [to] the memory are coupled; and

an address bus [coupled] to which the central processing unit, [to] the electrically programmable ROM and [to] the memory are coupled,

wherein [each of] the ROM and the memory are allocated in mutually different addresses in an address space of the central processing unit,

wherein the first program includes an instruction [which changes] to change a process of the CPU to a process [that controls] controlling a [writing] programming of the ROM based on the second program stored in the memory, and

wherein the second program includes an instruction [which returns] to return the CPU to the process based on the first program in the ROM after completion of the process that controls the writing of the ROM.

28. (Amended) A method of writing data into an electrically erasable programmable ROM (EEPROM) under control of a CPU [processing unit], wherein the EEPROM and the CPU [processing unit] are in a semiconductor substrate, the method comprising [the steps of]:

executing a first program in the EEPROM by the processing unit;

changing a process of the CPU [processing unit] executing the first program to a process [for] executing a second program stored in a memory[, which is] formed in the semiconductor substrate, when [the processing unit executes] an instruction in the first program is executed by the CPU;

executing the second program by the CPU [processing unit] in order to perform writing of data to the EEPROM by the CPU [processing unit] executing the second program; and

changing the process of the CPU [processing unit] executing the second program to the process [for] executing the first program when [the processing unit executes] an instruction in the second program is executed by the CPU,

wherein the memory and the EEPROM are disposed [allocated] in mutually different addresses in one address space of the CPU.

29. (Amended) A method of writing data into an electrically erasable programmable ROM (EEPROM) according to claim 28, wherein the CPU executes a jump instruction as said instruction in the first program, and

wherein the changing of the process of the processing unit is changed when the CPU [processing unit] executes a return instruction as said instruction in the second program.

30. (Amended) A method of writing data into an electrically programmable ROM under control of a central processing unit [CPU], wherein the electrically programmable ROM and the CPU are in a semiconductor substrate, the method comprising [the steps of]:

executing a first program in the electrically programmable ROM by the central processing unit;

changing a process of the CPU executing the first program to a process for executing a second program stored in

a mask ROM, which is formed in the semiconductor substrate, when [the CPU executes] a jump instruction in the first program is executed by the central processing unit;

executing the second program by the central processing unit [CPU] to perform writing to the electrically programmable ROM by the central processing unit [CPU] executing the second program; and

changing the process of the central processing unit [CPU] executing the second program to the process for executing the first program when [the CPU executes] a return instruction in the second program is executed by the central processing unit,

wherein the mask ROM [memory] and the electrically programmable ROM [EEPROM] are disposed [allocated] in mutually different addresses in one address space of the central processing unit.